REMARKS

Claims 1-26, 28-38, and 40-52 remain for consideration. The allowability of claims 3-5, 8-14, 16-18, 21-23, 25, 27-35, 39-42 and 49-51, and the allowance of claim 52 are acknowledged, and Applicants thank the Examiner for this recognition of patentable subject matter. The remaining claims are thought to be allowable over the cited art.

The amendments are made for the purpose of expediting prosecution and not for patentability, and the claim cancellations are made without prejudice. Applicants reserve the right to pursue subject matter of the original claims (prior to amendment) and subject matter of the canceled claims in subsequent prosecution.

The Office Action does not establish that claims 1-2, 15, 26, 38 and 45-46 are anticipated under 35 USC §102(b) by "Ong" (US patent number 5,821,772 to Ong et al.). The rejection is respectfully traversed because the Office Action fails to show that Ong teaches all the limitations of the claims.

Claim 1 includes, for example, limitations of and related to a configurable function unit including a configurable function unit component; at least one configurable decoder having decoder configuration data and a decoder output, the configurable decoder being operable to decode a value in data presented by the configurable function unit component; and wherein the configurable decoder is optimized to assert the decoder output based on a comparison of the decoder configuration data with the value presented by the configurable function unit component. These limitations are not shown to be taught by Ong.

The Office Action fails to show that Ong's counter corresponds to the claimed configurable function unit. There is no apparent configurability to Ong's counter. That is, Ong's counter is described as providing a count for addressing (col. 3, l. 6-10). There is no cited teaching that Ong's counter is configurable to perform any other than the fixed counting function. Thus, Ong's counter is not shown to be configurable and does not suggest the claimed configurable function unit.

The Office Action also fails to show that Ong's decoders correspond to the claimed configurable decoders. Ong's decoders DEC0 – DEC15 include XNOR

gates, AND gates, and address memory cells. Each decoder provides a high output signal responsive to the value output by the counter and an input address in the memory cells (col. 3, l. 11-24). There is no teaching cited that suggests Ong's decoders are configurable as claimed. That is, Ong's decoders appear to perform a fixed decoding function according to the XNOR and AND gates. Thus, Ong's decoders are not shown to be configurable and do not suggest the claimed configurable decoders.

Claim 2 is not shown to be anticipated by Ong. Claim 2 includes limitations of and related to the decoder configuration data being specified by configuring decoder cells having cell values of binary logic one, and binary logic zero, and the decoder output being asserted when the value presented by the configurable function unit component are consistent with the cell values. The Office Action cites the input data to Ong's decoders as suggesting these limitations. This alleged correspondence is clearly in error because the data input to Ong's decoders does not configure the function of the decoders as understood by those skilled in the art. Rather the decoders perform the fixed function on the input data. Thus, claim 2 is not shown to be anticipated.

Claims 15 and 19 depend from claim 1 and are not shown to be anticipated by Ong for at least the reasons set forth above.

Claim 26 is amended to include the limitations of claim 27, which is indicated as allowable and is now canceled. Claim 38 is amended to include the limitations of claim 39, which is indicated as allowable and is now canceled. The rejection of claims 26 and 38 is now moot.

Independent claim 45 includes limitations similar to those of claim 1. Thus, claim 45 is not shown to be anticipated for at least the same reasons as set forth above.

Claim 46 depends from claim 45 and includes limitations similar to those of claim 2. Thus, claim 46 is not shown to be anticipated by Ong as explained above.

Claims 47 and 48 depend from claim 45 and are not shown to be anticipated by Ong for at least the reasons set forth above for claim 45.

Therefore, the rejection of claims 1-2, 15, 19, 26, 38 and 45-48 should be withdrawn because the Office Action fails to show that Ong teaches all the limitations of the claims.

The Office Action fails to show that claims 6-7, 36-37 and 43-44 are unpatentable under 35 USC §103(a) over Ong in view of "New" (US patent no.6,288,570 to New (hereinafter "New"). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Ong with teachings of New, and fails to show that the combination could be made with a reasonable likelihood of success.

Claim 6 depends from claim 1, claim 36 depends from claim 26, and claim 43 depends from claim 38. Therefore, claims 6, 36, and 43 are not shown to be patentable for at least the reasons set forth above for claims 1, 26, and 38, respectively.

Claims 7, 37, and 44 also depend from claims 1, 26, and 38, respectively, and include limitations of and related to the integrated circuit being a complex programmable logic device (CPLD) having a plurality of function blocks, the function blocks including a plurality of macrocells. The Office Action fails to show that the Ong-New combination suggests these limitations. Those skilled in the art will recognize that an FPGA and a CPLD are structurally different types of programmable logic devices. Ong teaches an FPGA (Abstract), New also teaches an FPGA, and no showing is made that either of Ong or New suggests a CPLD. Therefore, the Office Action does not show that the Ong-New combination suggests the limitations of claims 7, 37, and 44.

The alleged motivation for combining New with Ong is improper in regards to claims 7, 37 and 44. The alleged motivation states that "it would have been obvious ... to implement the look-up tables of New in the logic block of Ong et al. to simplify implementation of a logic function." The alleged motivation is not supported by evidence because the claims involve CPLDs and neither of New nor Ong suggest the

structures within CPLDs as claimed. Thus, there would be no reason to combine the teachings to make a CPLD-type circuit as claimed.

Therefore, the rejection of claims 6-7, 36-37 and 43-44 over the Ong-New combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action fails to establish that claims 20 and 24 are unpatentable under 35 USC §103(a) over Ong in view of "Higashitsutsumi" (US patent no.5,226,063 to Higashitsutsumi). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Ong with teachings Higashitsutsumi, and fails to show that the combination could be made with a reasonable likelihood of success.

Claims 20 and 24 include limitations of and related to the configurable function unit component being a shift register or a feedback shift register.

The alleged motivation for combining Higashitsutsumi with Ong is conclusory, appears to render Ong nonfunctional, and is therefore improper. The alleged motivation states that "it would have been obvious ... to utilize the polynomial counter having shift registers with feedback of Higashitsutsumi in place of the counter of Ong et al. since it would provide a polynomial function." No evidence is presented to indicate why Ong's counter is deficient for its purpose. Nor is any evidence presented to indicate why one would substitute Higashitsutsumi's polynomial counter for Ong's counter.

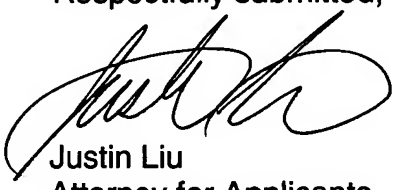
Ong's counter is used to enable addressing of configuration cells, and Higashitsutsumi teaches a polynomial counter implemented as a shift register (FIG. 5). Higashitsutsumi apparently uses the polynomial counter to remove noise from a signal. There is no apparent need for noise removal in Ong's addressing scheme. Furthermore, Higashitsutsumi's polynomial counter does not appear to permit proper addressing of Ong's configuration memory.

The rejection of claims 20 and 24 over the Ong-Higashitsutsumi combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patens, P.O. BOX 1450, Alexandria, VA, 22313-1450, on March 2, 2005.

Julie Matthews
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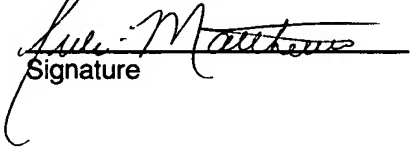

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